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AMENDED APPEAL BRIEF

Appl. No : 09/413,177 Conformation No.: 1672  
Applicant : Chan et al.  
Filed : 10/07/99  
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EXAMINER : Paul E. Brock II

Docket No. : CS99-107C  
Customer No.: 28112

Date : 02/24/06

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 08/12/04 and made FINAL, applicants filed a notice of appeal on 11/11/04. In accord with applicants' notice of appeal, please accept this amended appeal brief. No oral hearing is requested.

  
Stephen B. Ackerman, Reg. No 37,761

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 3, 2006.

Stephen B. Ackerman, Reg. No 37,761

Signature  3/3/06

AMENDED APPEAL BRIEF

1. Real Party in Interest

The real party in interest for this application is the assignee:

Chartered Semiconductor Manufacturing Ltd.  
60 Woodlands Industrial Park D  
Street 2  
Singapore 738406

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims:

Claims 1, 2, 5, 6, 8-18 and 22 are rejected. Claims 3, 4 and 7 are objected to. Claims 19-21 are cancelled. Claims 1, 2, 5, 6, 8-18 and 22 are being appealed.

4. Status of the Amendments:

The last amendment was made in response to the non-final Office Action of March 26, 2004, and was entered.

5. Summary of Claimed Subject Matter:

CLAIM 1 IS READ ON THE SPECIFICATION AND DRAWINGS AS  
FOLLOWS:

1. A method of forming air gaps within an integrated  
circuit structure, therewith forming a high quality  
inductor over a semiconductor substrate, comprising the  
steps of:

providing a semiconductor substrate, SEE FIGS. 1-13,  
UNDERLYING LAYER 10, THE SEMICONDUCTOR SUBSTRATE NOT  
HIGHLIGHTED, DESCRIPTION PAGE 23, LINES 6-10; with a  
partially fabricated integrated circuit structure, SEE FIG.  
1, ITEM 12, DESCRIPTION PAGE 12, LINES 3-21, PAGE 13, LINES  
1-11 having been created thereon and depositing a layer of  
dielectric SEE FIG. 1, ITEM 10, DESCRIPTION PAGE 12, LINES  
3-21, PAGE 13, LINES 1-11; over the semiconductor  
substrate;

forming a metal layer on said dielectric layer, SEE  
FIG. 1,  
ITEM 12, DESCRIPTION PAGE 13, LINES 13-21, PAGE 14, LINES  
1-4;

depositing a first thin layer of oxide over said  
dielectric layer, thereby including said metal layer, SEE

FIG. 2, ITEM 16, DESCRIPTION ON PAGE 14, LINES 21-24 AND ON PAGE 15, LINES 1-4;

forming a structure for first cavities over said first thin layer of oxide and aligned with said metal layer, said forming a structure for first cavities comprising applying and patterning

a first layer of disposable solid followed by applying and patterning a first layer of oxide, said patterning a first layer of oxide further comprising forming a first and a second opening

through said first layer of oxide, said first and second openings providing access to said first layer of disposable solid, SEE FIG. 3, ITEMS 22 AND 24, DESCRIPTION ON PAGE 14, LINES 21-24, AND PAGE 15, LINES 1-4, SEE FIG. 4, ITEM 18, DESCRIPTION ON PAGE 15, LINES 6-12, SEE FIG. 5, ITEM 20, DESCRIPTION ON PAGE 15, LINES 14-23, SEE FIG. 6, ITEM ??, DESCRIPTION ON PAGE 16, LINES 1-9;

forming a structure for second cavities above and aligned with said structure for said first cavities, said forming a structure for second cavities comprising applying and patterning a second layer of disposable solid followed by applying and patterning a second layer of oxide, said patterning a second layer of oxide further comprising forming a third and fourth opening through said second

layer of oxide, said third and fourth openings providing access to said second layer of disposable solid, thereby creating overlying patterned first and second layers of disposable solid separated by said first layer of oxide and interconnected by said first and second opening formed through said first layer of oxide, said overlying patterned first and second layers of disposable solid being accessible via said third and fourth opening formed through said second layer of oxide, SEE FIG. 7, ITEM 26, DESCRIPTION ON PAGE 16, LINES 11-17, 8, SEE FIG. 7, ITEM 28, DESCRIPTION ON PAGE 16, LINES 19-24 AND ON PAGE 17, LINES 1-2, SEE FIG. 9, ITEM 30, DESCRIPTION ON PAGE 17, LINES 4-11, SEE FIG. 10, ITEMS 32 AND 34, DESCRIPTION ON PAGE 17, LINES 13-23;

creating the first and the second cavities, SEE FIG. 11, ITEMS 36 AND 38, DESCRIPTION ON PAGE 18, LINES 1-11; performing an oxide deposition over said second cavities, creating a second thin layer of oxide, SEE FIG. 12, ITEM 32, DESCRIPTION ON PAGE 18, LINES 13-24 AND ON PAGE 19, LINES 1-2; and forming a metal inductor on said second thin layer of oxide, SEE FIG 13, ITEM 44, DESCRIPTION ON PAGE 19, LINES 4-24 AND ON PAGE 20, LINES 1-13;

(THIS COMPLETES FIGS. 1-13; SEE DESCRIPTION ON PAGE  
12 THROUGH PAGE 20)

6. Grounds of Rejection to be Reviewed upon Appeal

- Whether or not claims 1, 2, 5, 6, 15-17 and 22 under 35 U.S.C. 103(a) are patentable over Lur et al. (U.S. Patent 5,413,962) in view of Staudinger et al. (U.S. Patent 5,481,131)
- whether or not claims 8-12 under 35 U.S.C 103 are patentable over Lur et al. (US Patent 5,413,962) and Staudinger (US Patent 5,481,131) as applied to claim 1 above in view of Havemann et al. (US Patent 5,668,398)
- whether or not claims 13 and 18 under 35 U.S.C 103 are patentable over Lur et al. (US Patent 5,413,962) and Staudinger as applied to claim 1 above in view of Abidi et al. (US Patent 5,481,131), and
- whether or not claim 14 under 35 U.S.C 103 is patentable over Lur et al. (US Patent 5,413,962) and Staudinger as applied to claim 1 above in further in view of One of Ordinary Skill in the Art.

7. ARGUMENTS

7.1 ARGUMENTS addressing whether or not claims 1, 2, 5, 6, 15-17 and 22 under 35 U.S.C. 103(a) are patentable over Lur et al. (U.S. Patent 5,413,962) in view of Staudinger et al. (U.S. Patent 5,481,131).

Lur et al. (US Patent 5,413,962) provides for a multi-level electrode metal structure and the interconnecting inter-level metal studs used in the fabrication of VLSI circuits, in this respect therefore, Lur et al. or Staudinger et al. (U.S. Patent 5,481,131) or the combination thereof:

- do not provide for creating a high quality inductor on the surface of a silicon semiconductor substrate as claimed in claims 1, 15-18, 20 of the instant invention
- do not provide for an dielectric of air that surrounds interconnect metal
- do not provide for a number of overlying air gaps that are interconnected as claimed in claims 1 and 3-5 of the instant invention
- Lur et al. does not provide for oxide fins (36, 38, Fig. 13 of the instant invention) underneath the metal inductor 44;

the oxide fins of the instant invention provide support and stability for the overlying metal 44, simultaneously allowing horizontal air columns to exist underneath the inductor

- Lur et al. does not create an inductor (44, Fig. 13 of the instant invention) that overlies a upper layer of dielectric as claimed in claims 1 of the instant invention

- Lur et al. does not provide for openings (22, 24, 32 and 34, Fig. 13 of the instant invention) in layers of dielectric

through which nitride or any other disposable material can be removed as claimed in claims 3, 4, 5 of the instant invention

- Lur et al. does not provide for overlying layers of disposable material, such as nitride, interspersed with layers of dielectric as claimed in claims 1 and 3-5 of the instant invention

- the final construct that is provided by Lur et al. does not comprise horizontal air gaps (36, 38, Fig. 11 of the instant invention) between which horizontal layers of a dielectric are created, see Fig. 11 of the instant invention, and

- Lur et al. shows interconnect studs that connect to bit line and word lines of what appears to be a DRAM circuit configuration; gate electrodes are provided by Lur et al.; the instant invention is silent on this aspect of the Lur invention and is not limited to a DRAM device or the use of gate electrodes.

Regarding claims 1, 2 and 5 the following applies:

- the metal layer that is created by Lur et al., layer 26, Fig. 1, is connected to a source/drain region or to a gate electrode; the metal layer of the instant invention, layer 12, is not limited to being connected to a gate electrode
- the first layers of interconnect metal, layers 40, Fig. 1, that are created by Lur et al. connect to interconnect plugs 26; the instant invention does not create these first layers of interconnect metal
- Lur et al. deposits a number of thin envelop oxide layers such as layer 42, Fig. 1, layer 42, Fig. 2, layer 42, Fig. 4, layer 42, Fig. 6, layer 42, Fig. 8, layer 42, Fig. 9, layer 42, Fig. 10; all envelop layers have been referred

to by the number "42" by Lur et al., the multiplicity of layers has been deposited for the figures that have been referenced; the instant invention does not make use of such thin layers of oxide for protective purposes of the interconnect metal

- applicant respectfully disagrees with Examiner regarding the statement that Lur et al. creates, Figs. 2-4, a structure for

a first layer of cavities; Lur et al. does not make use of cavities but in contrast etches away the inter-level dielectric (col. 3, line 62) leaving an air dielectric 85, Fig. 11 of Lur et al.) between the electrode metal layers; an similar comment applies to Examiner's contention that Lur et al. creates a first and a second layer of cavities: the (only) cavity that is created by Lur et al. is cavity 85, shown in Fig. 11 where col. 3, lines 61 e.a.): "the inter-level dielectric is etched away". After the inter-level has been etched away, a (col. 3, lines 63 e.a.) "the surface of all electrode pattern metal and interlevel stud metal is covered with a coating of thin envelop oxide". Lur et al. provides an etch for the removal of the inter-level dielectric, which may be considered a standard procedure. Lur et al., therefore does not provide for the creation of

overlying layers of disposable solid, nor for the creation of access holes through layers of dielectric nor for the removal of the disposable solid through these access holes, nor for creating (as the instant invention does) overlying and interconnected air cavities.

Staudinger et al. provides for an Integrated Circuit having passive circuit elements but at no time does Staudinger et al. or Lur et al. or the combination thereof provide for or suggest the essential aspects of the instant invention that have been summarized *supra*, that is:

- forming a structure for a first layer of cavities
- forming a structure for a second layer of cavities above and aligned with the structure for the first layer of cavities,
- creating a first and a second layer of cavities, and
- forming a metal inductor overlying the created cavities.

Regarding claims 15-17, while many inductors are created having a spiral shape, not all inductors have a spiral shape. Since the inductor of the invention is created on the surface of a layer of dielectric, layer 42, Fig. 12,

the inductor of the invention is not limited to a spiral shape but can also be circular or polygonal in shape. This is specified in claims 15-17.

Regarding claim 17, the inductor 44 of the invention is created having very low parasitic capacitance between the inductor 44, Fig. 13, and a metal layer 12, Fig. 13. For this reason the inductor 44 can be created having a high inductive value and can at the same time be used for high frequency applications.

In other words: by providing the claimed invention it is now possible in the context of the claimed invention to create a high (inductive and Q) value, high frequency inductor. The layer or layers of material underlying the inductor is key and of the essence to these performance characteristics of the inductor. It must therefore be recognized and specified that, if an inductor is created using the claimed invention, this inductor can be a high inductive value, high frequency performance inductor as claimed in claim 18.

Regarding claim 22, Lur et al. provides for a layer 80, shown in the cross section of Fig. 11 of Lur et al., of passivation material, which is conventionally deposited over a created structure for the protection thereof.

This latter Lur et al. application bears no resemblance to the specification provided in claim 22 of the claimed invention, which specifies that the first layer and second layer of disposable solid are formed using nitride.

The Lur et al. application of nitride, as suggested for the layer 80 of passivation, is well known in the art and is as such not germane to the Lur et al. invention. The disposable solid of the claimed invention is used as part of a complex and complete processing sequence for the formation of air gaps within an integrated circuit structure. Two otherwise completely different processes cannot be equated for reasons of having one parameter in common, in this case the use of nitride, whereby however the nitride is used for entirely different purposes.

The above arguments can be summarized by stating that it would not be obvious to combine the teachings of Lur et al. with those Staudinger, since there is no suggestion or motivation in the teachings of any of the patents of the present invention.

The Lur et al. and the Staudinger inventions do not provide for the creation of horizontal air gaps that are interspersed with layers of dielectric while further these inventions do not provide for a method of removal of a disposable solid, such as nitride, for the creation of the air gaps as claimed in claims 1, 2, 5, 6 and 15-17 of the claimed invention.

None of the above-cited references address the invention as shown in the claims in which air gaps are created between overlying layers of dielectric. The invention is believed to be patentable over the prior art cited, as it is respectfully suggested that the combination of these various references cannot be made without reference to Applicant's own invention. None of the applied references address the problem of creating a high inductive value, high frequency inductor overlying a layer of metal.

Applicant has claimed his process in detail. The processes of Figs. 1-11, and the there-upon based and the there-from derived claims of the claimed invention, are believed to be both novel and patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one

skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination.

7.2 ARGUMENTS addressing whether or not claims 8-12 under 35 U.S.C 103 are patentable over Lur et al. (US Patent 5,413,962) and Staudinger (US Patent 5,481,131) as applied to claim 1 above in view of Havemann et al. (US Patent 5,668,398).

The relative merits of Lur et al. and Staudinger with respect to claim 1 have been discussed above and are

enclosed at this time by reference as being equally applicable to claims 8-12.

With respect to claim 8, this claim is a dependent claim to claim 1 and specifies that a polymer can be used for the first and second layers of disposable solid.

While Havemann teaches the use of a disposable solid that comprises a polymer, the claimed invention and the Havemann invention have no commonality in either the way that air gaps are created, the design and the there-from following cross

sections of the air gaps, the method in which the disposable solid is removed from the structure, and the like. The fact therefore that the disposable solid is commonly defined between Havemann and the claimed invention as being a polymer, while there is no further commonality between the claimed invention and the Havemann invention, cannot reasonably lead to the conclusion that one invention can be derived from the other invention, even by those who are skilled in the art.

It can in this respect and for purposes of comparison reasonably be asked whether two different cars, which have in common the use of a type of gas which is extracted from the gas tank, are by necessity the same cars or that the design and performance characteristics of one car is in any way related to the design and performance characteristics of the other car?

It is kindly suggested by Applicant that the same analogy between the Havemann and the claimed invention makes the use of a polymer by Havemann of no consequence in determining the uniqueness of the claimed invention.

With regard to claim 9, Havemann et al. teaches, col. 5, lines 49-67, that "the disposable solid layer 18 is removed through the porous dielectric layer 20 to form air gaps 22 as

shown in Fig. 1E." This latter process is performed by "exposing the wafer to oxygen or oxygen plasma, the oxygen moves through the porous dielectric layer 20 to reach the disposable solid layer 18 and react with the solid layer 18

and convert it to a gas that moves back out of the porous dielectric 20."

Claim 9 specifies creating a first and a second layer of cavities is heating the substrate in oxygen, evaporating the disposable solid layer using O<sub>2</sub> plasma.

Claim 9 however is a dependent claim to claim 1, which specifies, among others: "forming a structure for a first layer of cavities over the thin layer of oxide and aligned with the metal layer, the forming a structure for a first layer of cavities comprising applying and patterning a first layer of disposable solid followed by applying and patterning a first layer of oxide, the patterning a first layer of oxide further comprising forming a first and a second opening through the first layer of oxide.

From the above quote it is clear that the invention directly, by creating openings through the first layer of oxide,

provides a path for the removal of the disposable solid. Havemann does not provide for this but removes a solid through a more cumbersome process that has been detailed

above and that, in view of the method applied by Havemann et al., does not lead to as direct and as thorough a removal of the solid as is provided by the instant invention, whereby the removable solid can be directly attacked by oxygen resulting in evaporating the disposable solid layer using O<sub>2</sub> plasma. This process is easier to apply, more effective and provides more dependable (better removal of the disposable solid) results in creation an air filled space in the surrounding layer.

With regards to claim 10, this claim teaches that creating a first and a second layer of cavities is introducing a solvent to the substrate, dissolving the polymer (that is used as a disposable solid).

Applicant has carefully reviewed the text cited by Examiner in Havemann et al. invention with respect to claim 10, that is col. 5, lines 49-67 and col. 6, lines 15-25, but is, contrary to

Examiner's assertion, not able to locate any reference to the introduction of a solvent to the substrate.

Regarding claim 11, Havemann in the description of Figs. 5A through 5D, to which Examiner refers, the description of which is provided by Havemann in Col. 6, lines 43-76 and col. 7, lines 1-11 and not, as asserted by Examiner, in col. 5, lines 49-67, does provide for cavities between patterned layers of metal. First, Fig. 5A of Havemann, patterned and overlying layers 16/28 of metal and second oxide are created over first oxide layer 14. A disposable solid 18, Fig. 5B, is deposited, a porous dielectric 20 is deposited over the disposable solid 18 after which the disposable solid 18 is evaporated through the porous layer 20 of dielectric, creating cavities 22, Fig. 5D, between adjacent of metal traces and there-over deposited layers 24 of second oxide.

Claim 11 of the instant invention specifies heating the substrate to evaporate the polymer, thereby creating a first and a second layer of cavities. These layers of cavities are clearly shown in the cross sections of Fig. 11, elements 36 and 38. These cavities are not between patterned layers of metal and oxide but are created as an interconnected structure 36/38

within the dielectric layer 30, the interconnects being openings 22 and 24. This interconnected structure cannot, in its creation or in its final cross section, be compared with the openings 22,

Fig. 5D of Havemann for the reason that neither the creation nor the cross section have any commonality. The air gaps of the instant invention and the air gaps provided by Havemann et al. are created by removing a disposable solid, an opening is defined by the removable solid after which the removable is removed. Not in common between Havemann et al. and the instant invention are, among others, the process of the creation of the patterned layers of disposable solid, the cross sections of the created layers of disposable solid, the manner in which the disposable solid is removed, the layers that are adjacent to the created layers of disposable solid and the final structure, of which the air cavities form a part.

Havemann et al. does not, contrary to Examiner's assertion, provide for a first and a second layer of cavities, Havemann creates one layer of cavities surrounded by metal interconnects and overlying patterned layers of oxide.

Regarding claim 12, which specifies creating a first and a second layer of cavities by applying a vacuum to the substrate,

dissolving the polymer, the invention provided by Havemann does not provided for this method in essence because Havemann does not provide openings 32/34 and 22/24, shown in Fig. 11 of the instant invention, through which the disposable solid is directly accessible and through which the disposable solid can therefore directly be removed. Havemann et al. would, in applying as vacuum to the substrate, most likely destroy the porous layer 20, Fig. 5C, overlying the created air gaps.

While applicant acknowledges the teachings of Lur, Staudinger and Havemann et al. as cited by the Examiner, and although applicant does not necessarily agree that the Examiner's arguments show sufficient and proper basis for suggestion or motivation to modify or combine Lur, Staudinger and Havemann et al., applicant nonetheless also asserts that there is absent within the portions of Lur, Staudinger and Havemann et al. or any combination thereof,

as cited by the Examiner, an express or inherent teaching of each and every limitation within applicant's invention as taught and claimed within claims 8-12 of the instant invention.

Claims 8-12 are dependent claims to claim 1, neither Lur or Staudinger nor Havemann et al. nor any combination thereof

provide for the aspects of the instant invention that are specified in independent claim 1 of the invention on which claims 8-12 are based.

Specifically provided by the instant invention, aspects that are not provided by Lur nor Staudinger nor Havemann et al. or any combination thereof, are:

- forming a structure for a first layer of cavities over a thin layer of oxide and aligned with a metal layer, by applying and patterning a first layer of disposable solid followed by applying and patterning a first layer of oxide, thereby forming a first and a second opening through the first layer of oxide
- forming a structure for a second layer of cavities above and aligned with the structure for the first layer of

cavities by applying and patterning a second layer of disposable solid followed by applying and patterning a second layer of oxide thereby forming a first and a second opening through the second layer of oxide

- creating the first and the second layer of cavities
- performing an oxide deposition over the second layer of cavities, creating a thin layer of oxide, and
- forming a metal inductor on the thin layer of oxide.

To combine the teachings of Lur and Staudinger and Havemann et al. is not obvious, since there is no suggestion or motivation in the teachings of any of these patents of the present invention. The instant invention specifically provides a method of forming air gaps within an integrated circuit

structure and of forming a metal inductor on an upper thin layer of oxide. In the context of the instant invention, and not either supported by or inferred by or referred to by Lur and Staudinger and Havemann et al. singly or in combination thereof, provides a first and second layer of cavities, the cavities interconnected with openings, the second layer of cavities exposed through openings for easy

and complete removal of a created patterned layer of a disposable solid, over the surface of a substrate.

7.3 ARGUMENTS addressing whether or not claims 13 and 18 under 35 U.S.C 103 are patentable over Lur et al. (US Patent 5,413,962) and Staudinger as applied to claim 1 above in view of Abidi et al. (US Patent 5,481,131).

The relative merits of Lur et al. (US Patent 5,413,962) and Staudinger (US Patent 5,481,131) relating to claim 1 have been

discussed above and are enclosed at this time by reference as being equally applicable to claims 13 and 18.

Regarding claim 13, it is clear that an insulation layer, as specified by Abidi et al., can be used for multiple applications. In the case of the instant invention, the insulation layer is specified and provided in order to provide a more rugged construction that is protected from environmental impact during subsequent processing cycles. Without this protective layer the

inductor of the invention would be exposed and unprotected, resulting in a device that is prone to environmental damage.

Abidi et al. creates an inductor over a pit in a substrate and essentially shows the inductor as having a spiral shape. Other shapes are highlighted by Abidi et al., which however does not provide any commonality between Abidi et al. and the instant invention.

The essence of the instant invention is the creation of air gaps interspersed with layers of dielectric, Abidi does not

address these aspects of the instant invention. It must again be pointed out that, since the inductor of the instant invention is created overlying the surface of a layer of dielectric, this inductor is not in any way limited to the shape in which this inductor can be created. For this reason the various shapes in which an inductor can

be created must be specified in order to avoid incompleteness of the specification or the claims.

Regarding claim 18, the inductor of the invention is created having very low parasitic capacitance between the inductor 44, Fig. 13, and a metal layer 12, Fig. 13. For this reason the inductor can be created having a high inductive value and can at the same time be used for high frequency applications. In other words: by providing the invention it is now possible in the context of the instant invention to create a high value, high frequency inductor. The layer of material underlying the inductor is key and of the essence to these performance characteristics of the inductor. It must therefore be recognized and specified that, if an inductor is created using the instant invention, this inductor can be a high inductive value, high frequency performance inductor as claimed in claim 18. Without this claim it would not be clear just what could be accomplished using the invention.

The above arguments can be summarized by stating that it would not be obvious to combine the teachings of Lur et al. with those of Staudinger and Abidi et al., since there

is no suggestion or motivation in the teachings of any of the patents of the present invention.

None of these inventions provide for the creation of horizontal air gaps that are interspersed with layers of dielectric while further none of these inventions provide for a method of removal of a disposable solid, such as nitride, for the creation of the air gaps as claimed in the claims of the instant invention. None of the applied or known references address the invention as shown in the amended claims in which air gaps are created between overlying layers of dielectric.

The invention is believed to be patentable over the prior art cited, as it is respectfully suggested that the combination of these various references cannot be made without reference to Applicant's own invention.

None of the applied references address the problem of creating a high inductive value, high frequency inductor overlying a layer of metal. Applicant has claimed his process in

detail. The processes of Figs. 1-11 are believed to be both novel and patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art.

That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination.

7.4 ARGUMENTS addressing whether or not claim 14 under 35 U.S.C 103 is patentable over Lur et al. (US Patent 5,413,962) and Staudinger as applied to claim 1 above in further in view of  
One of Ordinary skill in the Art.

The relative merits of Lur et al. (US Patent 5,413,962) and Staudinger (US Patent 5,481,131) relating to claim 1 have been discussed above and are enclosed at this time by reference as being equally applicable to claim 14.

Claim 14 specifies that the partially fabricated integrated circuit structure comprising transistors being bipolar or CMOS devices interconnected to form an RF amplifier.

This aspect of the instant invention is not implied without the specific identification there-of as provided in claim 14. It

has been stated previously that, by providing the invention it is now possible in the context of the instant invention to create a high value, high frequency inductor.

Such an inductor, having high inductive and high Q values is most suited for application as a high frequency inductor for high-end performance devices. Such devices however can be created for a number of different applications, one of the preferred applications of the invention is that the inductor, created by the invention, as applied in combination with CMOS devices whereby these CMOS devices more specifically are interconnected to form an RF amplifier.

Claim 14, which is a dependent claim to claim 1, therefore limits the invention to a specific application, which represents an important market segment of semiconductor devices and which therefore requires to be specifically identified.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "SBA".

Stephen B. Ackerman (Reg. No  
37,761)

**CLAIMS APPENDIX**

The Claims outstanding in this application for United States Patent are as follows:

1. A method of forming air gaps within an integrated circuit structure, therewith forming a high quality inductor over a semiconductor substrate, comprising the steps of:

providing a semiconductor substrate with a partially fabricated integrated circuit structure having been created thereon and depositing a layer of dielectric over the semiconductor substrate;

forming a metal layer on said dielectric layer;

depositing a first thin layer of oxide over said dielectric layer, thereby including said metal layer;

forming a structure for first cavities over said first thin layer of oxide and aligned with said metal layer, said forming a structure for first cavities comprising applying and patterning a first layer of disposable solid followed by applying and patterning a first layer of oxide, said patterning a first layer of oxide further comprising

forming a first and a second opening through said first layer of oxide, said first and second

openings providing access to said first layer of disposable solid;

forming a structure for second cavities above and aligned with said structure for said first cavities, said forming a structure for second cavities comprising applying and patterning a second layer of disposable solid followed by applying and patterning a second layer of oxide, said patterning a second layer of oxide further comprising forming a third and fourth opening through said second layer of oxide, said third and fourth openings providing access to said second layer of disposable solid, thereby creating overlying patterned first and second layers of disposable solid separated by said first layer of oxide and interconnected by said first and second opening formed through said first layer of oxide, said overlying patterned first and second layers of disposable solid being accessible via said third and fourth opening formed through said second layer of oxide;

creating the first and the second cavities;

performing an oxide deposition over said second cavities, creating a second thin layer of oxide; and forming a metal inductor on said second thin layer of oxide.

2. The method of claim 1, wherein said forming a metal layer on said dielectric layer is forming a patterned layer of interconnect metal.

3. The method of claim 1 wherein said forming the structure for first cavities comprises the steps of:

    said applying said first layer of disposable solid over said first thin layer of oxide;

    said patterning said first layer of disposable solid comprising creating an opening in said first layer of disposable solid, whereby said opening in said first layer of disposable solid aligns with said metal layer;

    said applying said first layer of oxide includes depositing said first layer of oxide in said opening in said first layer of disposable solid, whereby said first layer of oxide has a dimension of thickness in addition to having a dimension of width; and

said patterning said first layer of oxide comprising creating a first and a second opening through said first layer of oxide, whereby said first and second openings through said first layer of oxide are located at opposite extremities of said first layer of oxide, whereby a distance between a center of said first and second openings through said first layer of oxide

is less than said dimension of width of said first layer of oxide.

4. The method of claim 1 wherein said forming the structure for second cavities comprises the steps of:

    said applying said second layer of disposable solid includes depositing said second layer of disposable solid in said first and second openings created in said first layer of oxide;

    said patterning said second layer of disposable solid comprises creating an opening in said second layer of disposable solid, whereby said opening in said second layer of disposable solid aligns with said metal layer and has a dimension when measured in a direction along said first layer of oxide that is approximately equal to a dimension

of the opening created in said first layer of disposable solid;

    said applying said second layer of oxide includes depositing said second layer of oxide in said opening created in said second layer of disposable solid, whereby said second layer of oxide has a dimension of thickness in addition to having a dimension of width; and

    said patterning said second layer of oxide comprising creating a third and fourth opening in said second layer of

oxide, whereby said third and fourth openings in said second layer of oxide are located at opposite extremities of said second layer of oxide, whereby a distance between a center of said third and fourth openings in said second layer of oxide is less than said dimension of width of said second layer of oxide.

5. The method of claim 1, said creating a first and a second layer of cavities is removing said first and second layer of disposable solid, said removal to take place by accessing said second layer of disposable solid by said third and fourth opening in said second layer of oxide, furthermore by accessing said first layer of disposable solid by said first and second openings in said first layer

of oxide, creating a first layer and a second layer of dielectric comprising horizontal oxide fins, further creating a first layer and a second layer of air gaps being interspersed with said first layer and a second layer of dielectric.

6. The method of claim 1 wherein said performing an oxide deposition over said second layer of cavities is creating a thin layer of oxide over said second layer of oxide, thereby furthermore closing said third and fourth openings created in said second layer of oxide.

7. The method of claim 1, creating additional layers of cavities over a preceding layer of cavities, said additional layers being created prior to performing an oxide deposition over an upper or last layer of cavities, said creation of additional layers of cavities comprising the steps of:

depositing an additional layer of disposable solid over a layer of oxide of a preceding layer of cavities, thereby including first and second openings created in said layer of oxide of a preceding layer of cavities;

creating an opening in said additional layer of disposable solid, said opening being aligned with said

metal layer and having a dimension when measured in a direction along said layer of oxide of a preceding layer of cavities that is approximately equal to a dimension of an opening created in a preceding layer of disposable solid;

depositing an additional layer of oxide over said additional layer of disposable solid, thereby including said opening created in said additional layer of disposable solid, said additional layer of oxide having a dimension of thickness in addition to having a dimension of width; and

creating a first and a second opening in said additional layer of oxide, said first and second openings being located at opposite extremes of said additional layer of oxide, a distance

between a center of said first and second openings being less than said dimension of width of said additional layer of oxide, creating a first layer and a second layer of dielectric comprising horizontal oxide fins, further creating a first layer and a second layer of horizontal air gaps being interspersed with said first layer and a second layer of dielectric.

8. The method of claim 1, said first and second layers of disposable solid comprising a polymer.

9. The method of claim 8, said creating a first and a second layer of cavities is heating said substrate in oxygen, evaporating said disposable solid layer using O<sub>2</sub> plasma.

10. The method of claim 8, said creating a first and a second layer of cavities is introducing a solvent to said substrate, dissolving said polymer.

11. The method of claim 8 wherein creating a first and a second layer of cavities is heating said substrate, evaporating said polymer.

12. The method of claim 11 wherein creating a first and a second layer of cavities is applying a vacuum to said substrate, dissolving said polymer.

13. The method of claim 1 wherein an insulating layer is deposited over said inductor thereby encapsulating said inductor.

14. The method of claim 1, said partially fabricated integrated circuit structure comprising transistors being bipolar or CMOS devices interconnected to form an RF amplifier.

15. The method of claim 1, said inductor being a spiral.

16. The method of claim 15, said spiral of said inductor being circular or polygonal.

17. The method of claim 16, the polygonal inductor being a square or a hexagon or an octagon.

18. The method of claim 1, said inductor having an inductance in excess of 1 nH and a self-resonance in excess of 10 MHz.

Claims 19-21: (cancelled).

22. The method of claim 1, said first layer of disposable solid and said second layer of disposable solid comprising nitride.

**EVIDENCE APPENDIX**

No evidence has been submitted pursuant to 37 CFR §§ 1.130, 1.131, or 1.132 nor are Applicants aware of any other evidence entered by the Examiner and relied upon by Applicant in the Appeal.

**RELATED PROCEEDING APPENDIX**

There are no related appeals or interferences for this  
United States Patent application.